CURRENT CLAIMS

1 - 33. (Cancelled).

34. (Previously Presented) A semiconductor device, comprising:

a semiconductor layer arranged on a main surface of a semiconductor substrate with an insulating layer between said semiconductor substrate and said semiconductor layer,

a plurality of MOS field effect transistors of a first conductivity type at a first active region of said semiconductor layer, and

a plurality of MOS field effect transistors of a second conductivity type at a second active region of said semiconductor layer,

wherein said first active region comprises a first partial isolation region including a first insulating layer,

said plurality of MOS field effect transistors of the first conductivity type being isolated from each other by said first partial isolation region,

said second active region including a second partial isolation region including a second insulating layer,

said plurality of MOS field effect transistors of the second conductivity type being isolated from each other by said second partial isolation region,

further comprising a perfect isolation region including a third insulating film provided between said first active region and said second active region, said perfect isolation region also in contact with said insulating layer,

said first active region and said second active region being electrically isolated from each other by said perfect isolation region,

said semiconductor layer located at said first active region having a film thickness identical to the film thickness of said semiconductor layer located at said second active region,

a lower portion of said semiconductor layer located at said first active region is provided under said first insulating film as a first lower semiconductor layer, each portion of said semiconductor layer located at said first active region being electrically connected with each other integrally by said first lower semiconductor layer,

a lower portion of said semiconductor layer located at said second active region is provided under said second insulating film as a second lower semiconductor layer, each portion of said semiconductor layer located at said second active region being electrically connected with each other integrally by said second lower semiconductor layer,

wherein an electrode is provided in respective semiconductor layers of said first active region and said second active region, and

each said electrode is held at a ground potential or a predetermined fixed potential.

35. (Cancelled)

36. (Previously Presented) The semiconductor device according to claim 34, wherein a field shield gate electrode is provided above said first partial insulating layer in said first isolation region.

37. (Previously Presented) The semiconductor device according to claim 34, wherein at least a portion of said first insulating film in said first partial isolation region is an oxide film made by local oxidation of said semiconductor layer.

38. (Previously Presented) The semiconductor device according to claim 34, wherein said third insulating film in said perfect isolation region is a replacement for said semiconductor layer in said perfect isolation region completely removed.

39. (Previously Presented) The semiconductor device according to claim 38, wherein at least a portion of said third insulating film in said perfect isolation region is an oxidation of all said semiconductor layer in said perfect isolation region.

40. (Previously Presented) The semiconductor device according to claim 38, wherein at least a portion of said third insulating film in said perfect isolation region is an insulating film identical to an interlayer insulating film provided above said MOS field effect transistor of the first conductivity type or said MOS field effect transistor of the second conductivity type.

41. (Previously Presented) The semiconductor device according to claim 38, wherein at least a portion of said third insulating film in said perfect isolation region is a multilayered insulating film having a plurality of insulating films stacked.

42. (Previously Presented) The semiconductor device according to claim 41, wherein at least one layer of said insulating films forming said multilayered insulating film is a film formed prior to formation of a gate electrode of said MOS field effect transistor of the first conductivity type and a gate electrode of said MOS field effect transistor of the second conductivity type.

43. (Previously Presented) The semiconductor device according to claim 42, wherein said first insulating film in said first partial isolation region is a gate insulating film on which a field shield gate electrode is provided, and

one of said insulating films forming said multilayered insulating film is a sidewall formed simultaneous to formation of a sidewall provided at said field shield gate electrode, and is formed at a sidewall of said first active region and said second active region.

44. (Previously Presented) The semiconductor device according to claim 41, wherein at least one of said insulating films forming said multilayered insulating film is a film formed after forming gate electrodes of

said MOS field effect transistors of the first conductivity type and said MOS field effect transistor of the second conductivity type.

45. (Cancelled)